What is claimed is:

1. A digital-to-analog converter circuit that is arranged to drive a capacitive load, the circuit comprising:

a current digital-to-analog converter that is configured to provide a first current to a sense node in response to a digital input signal, wherein the current digital-to-analog converter is coupled to a first power supply node;

a first resistance circuit that is coupled between the sense node and a second power supply node;

a second resistance circuit that is coupled between the sense node and an output node; and

an amplifier circuit having a first amplifier input, a second amplifier input, and an amplifier output, wherein the amplifier circuit is configured to receive a reference signal at the first amplifier input, the second input is coupled to the sense node, the amplifier output is coupled to the output node, the amplifier circuit is arranged such that the voltage associated with the sense node is approximately constant when steady state conditions are reached, the amplifier circuit is further coupled to a local power supply node, and wherein the local power supply node has a voltage that is higher than a voltage that is associated with the first supply node relative to the second power supply node.

2. The digital-to-analog converter circuit of Claim 1, wherein the first resistance circuit comprises at least one of a first resistor and a transistor that is biased as a resistor, the second resistance circuit comprises at least one of a second resistor and a transistor that is biased as another resistor, wherein the first and second resistance circuits are matched types.

3. The digital-to-analog converter circuit of Claim 1, wherein the voltage associated with the local power supply of the amplifier circuit is provided by a charge pump circuit in response to the voltages associated with the first power supply node and the second power supply node.

4. The digital-to-analog converter circuit of Claim 1, wherein the amplifier circuit comprises:

a differential pair; and

a load circuit, wherein the load circuit is coupled to the local power supply node.

5. The digital-to-analog converter circuit of Claim 1, wherein the amplifier circuit comprises:

a differential pair;

a current mirror load comprising first and second transistors;

a third transistor that is configured to operate as a cascode transistor in cooperation with the first transistor; and

a fourth transistor that is configured to operate as a cascode transistor in cooperation with the second transistor.

6. The digital-to-analog converter circuit of Claim 5, the amplifier circuit further comprising a third resistance circuit, wherein the third resistance circuit is coupled between the gate of first transistor and the gate of the third transistor.

7. The digital-to-analog converter circuit of Claim 1, the amplifier circuit further comprising:

a differential pair comprising first and second transistors;

a third transistor that is configured to operate as a cascode transistor in cooperation with the first transistor;

a fourth transistor that is configured to operate as a cascode transistor in cooperation with the second transistor; and

a load circuit, wherein the load circuit is coupled to the local power supply node.

8. The digital-to-analog converter circuit of Claim 7, the amplifier circuit further comprising:

a fifth transistor having a gate that is coupled to the gate of the third and fourth transistors, a source that is coupled to the source of the first and second transistors, and a drain that is coupled to the gate of the fifth transistor, wherein the fifth transistor is configured such that a gate to source voltage of the fifth transistor is significantly greater than a gate to source voltage of the first transistor; and

a current-limiting device that is coupled between the first supply node and the drain of the fifth transistor.

9. The digital-to-analog converter circuit as in Claim 8, wherein the current-limiting device comprises one of a fourth resistance circuit and a first current source circuit.

10. The digital-to-analog converter circuit of Claim 1, wherein the amplifier circuit comprises:

a first transistor having a first gate, a first source, and a first drain, wherein the first gate corresponds to the first amplifier input;

a second transistor having a second gate, a second source, and a second drain, wherein the second source is coupled to the first source, and the second gate corresponds to the second amplifier input;

a third transistor having a third gate, a third source, and a third drain, wherein the third source is coupled to the first source, and the third drain is coupled to the third gate;

a fourth transistor having a fourth gate, a fourth source, and a fourth drain, wherein the fourth source is coupled to the first drain, and the fourth gate is couple to the third gate;

a fifth transistor having a fifth gate, a fifth source, and a fifth drain, wherein the fifth gate is coupled to the fourth gate, and the fifth source is coupled to the second drain;

a sixth transistor having a sixth gate, a sixth source, and a sixth drain, wherein the sixth gate is coupled to the fourth drain;

a third resistance circuit that is coupled between the fourth drain and the sixth drain;

a seventh transistor having a seventh gate, a seventh source, and a seventh drain, wherein the seventh drain is coupled to the fifth drain, and the seventh gate is coupled to the sixth gate;

a eighth transistor having a eighth gate, a eighth source, and a eighth drain, wherein the eighth drain is coupled to the sixth source, and the eighth source is coupled to the local power supply node;

a ninth transistor having a ninth gate, a ninth source, and a ninth drain, wherein the ninth source is coupled to the eighth source, and the ninth drain is coupled to the seventh source;

a fourth resistance circuit that is coupled between the third drain and the first power supply node; and

a first current source circuit that is coupled between the first source and the second power supply node.

11. A digital-to-analog converter circuit that is arranged to provide an output voltage to a capacitive load in response to a digital input signal, the circuit comprising:

a current digital-to-analog converter that is arranged to provide a first current to a sense node in response to the digital input signal, wherein the current digital-to-analog converter is coupled to a first power supply node such that the first current is sourced from a voltage that is associated with the first power supply node;

a first means for providing that is configured to provide a second current in response to a sense voltage and a reference voltage, wherein the sense voltage is associated with the sense node, the means for providing has a local power supply voltage that corresponds to a local power supply node, the local supply voltage is higher than the voltage that is associated with the first power supply node relative to a voltage associated with a second power supply node, at least part of the second current is sourced from the local power supply voltage, and wherein the first means for providing is configured to couple at least part of the second current to the sense node; and

a first means for converting that is configured to convert a sum of the first and second currents to the sense voltage, wherein the output voltage is limited by the local supply voltage.

12. The digital-to-analog converter circuit of Claim 11, further comprising a charge pump circuit, wherein the charge pump circuit is arranged to provide the local power supply voltage in response to the voltage associated with the first power supply node and the voltage associated with the second power supply node.

13. The digital-to-analog converter circuit of Claim 11, wherein

the first means for converting is coupled between the sense node and the second power supply node; and

wherein the first means for providing comprises:

a second means for converting that is coupled between the sense node and an output node;

a means for amplification having a first amplifier input, a second amplifier input, and an amplifier output, wherein the means for amplification is configured to receive the reference signal at the first amplifier input, the means for amplification is further configured to receive the sense voltage at the second amplifier output, and the amplifier output is coupled to the output node, the amplifier circuit is arranged such that the sense voltage is approximately constant when steady state conditions are reached, and wherein the amplifier circuit is further coupled to the local power supply node.

14. The digital-to-analog converter circuit of Claim 13, wherein the first means for converting comprises at least one of a first resistor and a transistor that is biased as a resistor, the second means for converting comprises at least one of a second resistor and a transistor that is biased as another resistor, wherein the first and second means for converting are matched types.

15. The digital-to-analog converter circuit of Claim 11, wherein the means for amplification comprises:

a differential pair;

a second means for providing that is configured to provide a tail current; and

a load circuit, wherein the load circuit is coupled to the local power supply node.

16. A method for producing an analog voltage with a capacitive load in response to a digital input signal, the method comprising:

providing a first current in response to a digital input signal such that the first current is sourced from a voltage that is associated with a first power supply node;

coupling the first current to a sense node;

providing a second current in response to a sense voltage and a reference voltage such that at least part of the second current is sourced from a voltage associated with a local power supply node, wherein the voltage that is associated with the local power supply node is higher than the voltage that is associated with the first supply node relative to a second power supply node;

coupling at least a portion of the second current to the sense node; and

converting the sum of the first and second currents to the sense voltage, wherein the analog voltage is limited by the voltage associated with the local supply node.

17. The method of Claim 16, further comprising providing the voltage associated with the local power supply node, wherein providing the voltage is accomplished via a charge pump circuit that is responsive to the voltage associated with the first power supply node and the voltage associated with the second power supply node.

18. The method of Claim 16, wherein providing the first current comprises performing a current digital-to-analog conversion.

19. The method of Claim 16, wherein converting the sum is accomplished via a resistance circuit that is coupled between the sense node and the second supply node, and wherein coupling the second current to the sense node comprises providing the second current to an output node, wherein the analog voltage is associated with the output node, and wherein the output node is coupled to the sense node via another resistance circuit that is coupled between the output node and the sense node.

20. The method of Claim 16, wherein providing the second current comprises providing the second current such that the second current is approximately proportional to the difference between the reference voltage and the sense voltage.